

A Comprehensive Review of Low-Power, Low-Delay Domino Logic Techniques in CMOS VLSI

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ABSTRACT

Domino logic is widely employed in high-speed VLSI circuits due to its fast-switching capability and reduced area compared to static CMOS logic. However, conventional domino logic suffers from high dynamic power consumption, increased leakage current, and contention-induced delay, particularly in deep submicron and nanometre technologies. Clock keeper circuits are commonly used to improve noise immunity and maintain the dynamic node during the evaluation phase, but improper keeper design can significantly degrade power and performance. This paper presents a comprehensive review of low-power, low-delay, and low-leakage clock keeper domino logic techniques reported in the literature. Existing approaches are systematically classified based on keeper control strategies, contention reduction methods, and leakage mitigation techniques. A qualitative comparison of these designs is performed using key performance metrics such as power dissipation, propagation delay, leakage current, and noise immunity.

Keywords : Domino Logic , CMOS Low Power VLSI, Wide Fan-In Gates, Leakage Reduction, High-Speed Circuits

I. INTRODUCTION

Domino logic is widely employed in high-speed VLSI systems such as microprocessors, arithmetic units, and memory interfaces due to its fast-switching speed, reduced transistor count, and high performance compared to static CMOS logic. The dynamic nature of domino logic enables rapid evaluation, making it attractive for deep submicron and nanometre-scale integrated circuits where performance is critical.

Despite these advantages, conventional domino logic suffers from several significant challenges. High dynamic power consumption occurs due to frequent charging and discharging of the dynamic node. As technology scales, leakage current becomes a dominant concern, leading to increased static power dissipation and potential loss of stored charge at the dynamic node. In addition, contention between the pull-down network and the keeper transistor during the evaluation phase introduces propagation delay and further increases power consumption. These issues limit the widespread use of domino logic in low-power and energy-efficient applications.

To enhance the robustness of domino logic circuits, clock keeper transistors are commonly employed. The keeper maintains the logic state of the dynamic node during the evaluation phase by compensating for leakage and noise-induced charge loss. However, improper keeper design can result in increased contention current, degraded performance, and higher power dissipation. As a result, numerous clock keeper domino logic techniques have been proposed to achieve low power consumption, reduced delay, and minimized leakage current while maintaining adequate noise immunity.

This paper reviews recent clock keeper domino logic techniques reported in the literature, focusing on low-power, low-delay, and low-leakage design approaches.

II. LITERATURE REVIEW

Kosuri Bhavani et al. [1] proposed a comparator-based domino logic technique for wide fan-in dynamic gates to reduce power consumption and propagation delay. The design addresses leakage and contention issues present in conventional footed and footer less domino logic structures. Compared to existing foot-driven stack transistor domino logic, the proposed technique achieves improved power and delay performance, at the cost of increased circuit complexity.

Sumit Sharma et.al [2] proposed a novel low-power domino logic technique that provides static output during the evaluation phase for high-frequency changing inputs. The authors addressed a key limitation of conventional domino logic, where the dynamic node cannot be recharged once discharged during evaluation, leading to incorrect operation for rapidly changing inputs. By modifying the keeper circuit using a footer transistor and a

current mirror structure, the proposed design achieves improved power dissipation, reduced delay, and better power-delay product compared to existing domino logic techniques. However, the use of additional circuitry increases design complexity.

Alok Kumar Singh et.al [3] analyzed and modified Constant Delay (CD) logic to improve speed and power efficiency in dynamic CMOS circuits. The authors evaluated multiple CD logic-based circuits using 90 nm CMOS technology and compared performance metrics such as power consumption, delay, power-delay product, and noise. Simulation results showed that CD logic achieves reduced delay and improved speed compared to conventional domino logic, making it suitable for high-speed applications. However, the reliance on clocked dynamic operation and switching activity limits its effectiveness for low-power designs.

Sandeep Garg et al. [4] proposed a noise-immune domino logic design employing silicon nanomaterials to improve the robustness of wide fan-in gates. The study addresses the increase in leakage current and reduced noise immunity that occurs in conventional wide fan-in domino gates due to scaling of supply and threshold voltages in nanoscale CMOS technology. By using NMOS transistor stacking and an optimized keeper design, the proposed method reduces both dynamic and leakage power, resulting in improved noise tolerance and reduced propagation delay. Compared to existing techniques such as CPVT, CMFD, MCS-D, and CEDL, the proposed approach achieves significant reductions in power, delay, and power-delay product, although the increased footer transistor width leads to larger area overhead.

Balaji Ramakrishna S et.al [5] proposed a high-performance robust keeper design technique (ATKDB) for wide fan-in domino OR logic using 16 nm CNTFET technology. The study addresses power consumption, propagation delay, and charge-sharing issues that commonly arise in wide fan-in domino circuits. By employing a modified keeper with variable threshold voltage and a dynamic foot buffer, the design reduces contention current, minimizes clock loading, and maintains the dynamic node at logic high during evaluation. Simulation results demonstrate substantial reductions in power, delay, and power-delay product (PDP) compared to conventional domino techniques, while ensuring glitch-free operation for 16- and 32-input OR gates. However, the inclusion of a body-bias generator increases the transistor count slightly.

Balasubramanian et al. [6] proposed a CHSK-CCD domino logic technique to improve robustness, reduce power consumption, and enhance noise immunity in wide fan-in domino circuits. The study addresses challenges in conventional domino logic such as leakage current, charge sharing, and contention current, which degrade speed and reliability. By combining CHSK logic with Complementary CMOS Domino (CCD) design, the proposed circuit minimizes leakage, improves unity noise gain, and reduces propagation delay. Simulation results demonstrate improved power, delay, power-delay product, and noise performance compared to existing techniques, although increased keeper sizing slightly affects circuit area.

Sandeep Garg et.al [7] proposed a low-power domino logic design for deep-submicron CMOS technology that addresses leakage, delay, and noise immunity issues in wide fan-in gates. The study identifies challenges in conventional domino logic, such as increased sub-threshold leakage and gate leakage due to technology scaling, which degrade circuit performance at high frequencies. By stacking NMOS transistors in the proposed FDSTDL technique, the design achieves reduced leakage power, improved noise performance, and lower propagation delay. Comparative analysis with existing domino techniques shows up to 59.47% power reduction, 44.6% delay reduction, and improved unity noise gain, demonstrating enhanced efficiency, although device sizing variability must be carefully managed.

Nor Fatin Izzati Rajuli et al. [8] investigated the impact of Negative Bias Temperature Instability (NBTI) on the performance of domino logic circuits in nanoscale CMOS designs. The study addresses reliability challenges caused by threshold voltage (V_{th}) shifts in PMOS transistors under negative bias at elevated temperatures, which increase propagation delay and degrade circuit speed. Using simulation tools such as TCAD, the authors analyzed different NBTI defect mechanisms and stress conditions, highlighting the effect of temperature and stress duration on average power consumption and delay degradation. The results show that circuits are most sensitive to prolonged stress times and Nit-only defect mechanisms, emphasizing the importance of considering aging effects and reliability in low-power domino logic design, although mitigation strategies may increase design complexity.

Dr. M. Chennakesavalu et al. [9] proposed the Low-Leakage Clock Keeper Domino Logic (LLCKDL) technique for CMOS logic gates to reduce leakage power, improve noise immunity, and enhance propagation speed in large fan-in circuits. The design addresses challenges in conventional dynamic and domino logic, including charge leakage, keeper contention, and subthreshold power dissipation, which degrade performance at high frequencies. By stacking transistors efficiently and optimizing keeper sizing, the proposed LLCKDL method reduces power consumption by up to 76.47%, minimizes delay by up to 56.94%, and improves power-delay and energy-delay products compared to existing designs. While the approach increases design complexity slightly, it demonstrates superior performance for low-power, high-speed CMOS applications.

Sapna Rani Ghimiray et.al [10] proposed a Stack-Scheme Clocked-Bleeder Domino (SS-CBD) technique for low-leakage, wide fan-in dynamic logic applications, focusing on high-speed 40-bit tag comparators. The study

addresses challenges in conventional domino logic, including high dynamic power due to voltage swings at the dynamic node, sub-threshold leakage, and reduced noise immunity in wide fan-in gates. By employing stack transistors and clocked-bleeder circuitry, the SS-CBD method limits voltage swing, reduces leakage, and improves gate speed while maintaining consistent noise immunity. Simulation results demonstrate up to 58% power savings and approximately 10.8% speed improvement compared to prior designs, making the approach effective for low-power, high-speed cache memory applications.

Karthikeyan et al. [11] proposed a leakage reduction charge-pump-based domino logic technique for high fan-in VLSI circuits to improve speed and reduce power consumption. The study addresses challenges in conventional domino logic, including leakage currents, high dynamic power, and keeper contention, which degrade performance in deep-submicron technologies. By integrating a charge pump to boost node voltage and an additional NMOS transistor to suppress leakage, the proposed technique reduces delay, leakage power, and the power-delay product for wide fan-in gates. Simulation results demonstrate improved speed and energy efficiency compared to standard domino OR logic, high-speed domino logic, and lector-with-footed-diode designs, making it suitable for low-power, high-speed applications.

Suresh Sahadeorao Gawande et.al [12] proposed a leakage-tolerant, high-performance wide fan-in domino logic circuit to improve robustness and noise immunity in low-power VLSI designs. The study addresses challenges in conventional wide fan-in domino circuits, where increased parallel evaluation paths lead to higher leakage and degraded noise immunity. The proposed design optimizes the keeper transistor sizing to balance the trade-off between noise immunity, power consumption, and evaluation delay. Simulation results for an 8-input OR gate using a 65 nm PTM CMOS model demonstrate a 97% reduction in power-delay product (PDP) with a 7% increase in delay, and an improvement in unity noise gain (UNG) from 1.15 to 1.26. The technique is suitable for high-speed embedded processors requiring low power consumption while maintaining robust noise performance.

Dr. Anita Angeline A et al. [13] proposed an NMOS-based dynamic logic design for high-speed circuits, improving domino logic performance in terms of power-delay product, noise immunity, and propagation delay. The design addresses issues like charge-sharing and leakage at the dynamic node, common in conventional domino circuits. Comparative results show better PDP than footless domino logic, with potential for further optimization in noise margin, area, and energy-delay product for high-performance applications such as processors and decoders.

Shiksha and Kamal et.al [14] proposed a new domino logic design aimed at improving power-delay product and noise immunity. The design addresses leakage, charge sharing, and sub-threshold current issues common in conventional domino logic. By adjusting the threshold voltages and employing stacked NMOS or inverter-based techniques, the circuit achieves better speed, reduced power-delay product, and improved noise margin with minimal additional circuitry. Simulations on 90 nm CMOS technology demonstrate its suitability for high-speed, low-power embedded processors.

Uday Kumar Rai et.al [15] presented a low-power, high-speed NP (Zipper/NORA) Domino CMOS design. This approach overcomes the instability, charge-sharing, and leakage issues of conventional Domino CMOS while reducing transistor count and area. The NP Domino circuit provides both inverting and non-inverting outputs, supports pipelined operation, and achieves high speed even at low supply voltages (~320 mV). The design demonstrates significantly lower energy-delay product and is suitable for low-voltage, high-speed arithmetic circuits like full adders.

Manish Tiwari et.al [16] proposed a novel Nodal State Comparison-based Dynamic Hold (NSC-DH) technique for low-power OR gates in domino logic. The technique focuses on minimizing leakage and dynamic power in wide fan-in OR gates by dynamically monitoring the state of the evaluation node and controlling the keeper transistor accordingly. By selectively holding the dynamic node only when required, it reduces contention currents and unnecessary switching, improving energy efficiency. Simulation results demonstrate that NSC-DH achieves lower power consumption, improved noise immunity, and reduced delay compared to conventional domino OR gate designs, making it suitable for low-power, high-performance VLSI applications.

Volkan Kursun et.al [17] paper proposes a variable strength keeper (VSK) for CNTFET-based domino logic to reduce leakage, improve noise immunity, and enhance speed. By dynamically adjusting keeper strength, the design minimizes contention during evaluation and maintains logic integrity during precharge. Simulations show lower power, reduced delay, and improved energy-delay product, making it suitable for high-speed, low-power VLSI circuits, especially wide fan-in gates.

Kumar et.al [18] The study on charge sharing fault detection for CMOS domino logic circuits addresses the reliability issue where charge redistribution among series transistors unintentionally discharges the dynamic node, leading to incorrect logic evaluation and degraded noise immunity. The paper proposes a fault detection mechanism that identifies conditions under which charge sharing occurs, enabling adaptive control of keeper or evaluation circuitry to mitigate errors. Simulation results indicate that this detection scheme enhances overall circuit robustness and reduces fault rates compared to conventional domino logic, although it introduces additional monitoring circuitry overhead.

Pranab Kishore Dutta et.al [19] This paper presents a contention-aware stacking-based domino logic technique aimed at improving performance in wide fan-in gates while reducing leakage and overall power consumption. The proposed design addresses the contention current problem between keeper and evaluation transistors by employing a stacked transistor configuration, which effectively suppresses unwanted discharge of the dynamic node. Simulation results demonstrate significant reductions in leakage power and improved noise immunity, along with enhanced circuit robustness for large fan-in implementations, making it suitable for high-speed low-power VLSI applications. by adding all thses do a table and technique used in that

Ref.	Author(s)	Technique Used	Key Contribution (Short)
[1]	Kosuri Bhavani et al.	Comparator-Based Domino Logic	Reduces leakage and contention in wide fan-in gates with improved power and delay
[2]	Sumit Sharma et al.	Static Output Domino with Modified Keeper	Enables correct operation for high-frequency inputs with better PDP
[3]	Alok Kumar Singh et al.	Modified Constant Delay (CD) Logic	Improves speed and delay consistency for high-speed dynamic circuits
[4]	Sandeep Garg et al.	NMOS Stacking with Optimized Keeper	Enhances noise immunity and reduces leakage in nanoscale domino logic
[5]	Balaji Ramakrishna S et al.	ATKDB Keeper (CNTFET-Based)	Variable-threshold keeper reduces contention and PDP for wide fan-in OR gates
[6]	Balasubramanian et al.	CHSK-CCD Domino Logic	Combines CHSK and CCD to improve robustness and noise performance
[7]	Sandeep Garg et al.	FDSTD (Stacked NMOS Domino)	Achieves low leakage and improved unity noise gain in deep-submicron CMOS
[8]	Nor Fatin Izzati Rajuli et al.	NBTI Reliability Analysis	Analyzes aging effects on delay and power in domino logic circuits
[9]	M. Chennakesavalu et al.	LLCKDL (Low-Leakage Clock Keeper)	Reduces leakage, delay, and PDP using optimized keeper stacking
[10]	Sapna Rani Ghimiray et al.	SS-CBD (Clocked-Bleeder Domino)	Limits voltage swing to reduce leakage and improve speed
[11]	Karthikeyan et al.	Charge-Pump-Based Domino Logic	Improves speed and reduces leakage using boosted node voltage
[12]	Suresh S. Gawande et al.	Optimized Keeper Sizing Domino	Enhances noise immunity with significant PDP reduction
[13]	Anita Angeline A et al.	NMOS-Based Dynamic Domino	Improves PDP and reduces charge-sharing effects
[14]	Shiksha & Kamal Kant Kashyap	Threshold-Controlled Domino Logic	Improves noise margin and speed with minimal hardware overhead
[15]	Uday Kumar Rai et al.	NP (Zipper/NORA) Domino Logic	Enables low-voltage, high-speed operation with reduced transistor count
[16]	Manish Tiwari et al.	NSC-DH (Dynamic Hold Technique)	Adaptive keeper control reduces leakage and contention
[17]	Volkan Kursun et al.	Variable Strength Keeper (CNTFET)	Dynamically adjusts keeper strength for low power and high speed
[18]	Kumar et al.	Charge Sharing Fault Detection	Detects and mitigates charge-sharing-induced logic failures
[19]	Pranab Kishore Dutta et al.	Contention-Aware Stacked Domino	Suppresses contention current and leakage in wide fan-in gates

III. CONCLUSION

From the analysis of 20 research papers on domino logic circuits, it is evident that significant progress has been made in achieving high-speed, low-power, and robust wide fan-in logic designs. Key insights include the importance of keeper transistor optimization, stacking techniques, charge-sharing mitigation, and dynamic node control to reduce leakage and enhance noise immunity. Advanced methods such as NP Domino structures, CHSK-CCD integration, LLCKDL, charge-pump-based designs, and emerging technologies like FINFETs and CNTFETs have consistently shown improvements in power-delay product, energy efficiency, and circuit reliability.

The overall trend indicates a shift toward low-voltage operation, dynamic control of keeper and evaluation networks, and use of novel transistor technologies to meet the demands of modern high-performance and portable digital systems. These techniques collectively balance the trade-offs between speed, power, noise immunity, and circuit area.

Motivation : For future work, there is a strong motivation to explore hybrid approaches combining novel materials (CNTFETs, FinFETs), advanced pipelined architectures, and AI-assisted design optimization. Such strategies could further enhance low-power, high-speed, and reliable domino logic circuits for next-generation VLSI and embedded applications.

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