

Retention of H.266 High Efficiency Video Coding (HEVC)

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ABSTRACT

This paper provides an extensive analysis and summary of High Efficiency Video Coding (HEVC). It offers a comprehensive understanding of the analytical and predictive procedures defined in the latest video coding standard introduced by the ITU-T Video Coding Experts Group and ISO/IEC MPEG, thereby contributing to the field of video processing. The study also discusses various algorithms and architectural requirements for implementation, including techniques such as parallelism, pipelining, finite state machines (FSM), and other related methods.

Keywords: HEVC, Video Compression, Video Coding Standards, ITU-T VCEG, ISO/IEC MPEG, Video Processing, HEVC Algorithms

INTRODUCTION

The rapid advancement of multimedia technologies, ultra-high-definition video formats, and real-time streaming applications has created a growing demand for highly efficient video compression standards. Modern applications such as 4K/8K video streaming, virtual reality, video conferencing, and immersive media require high visual quality at reduced bandwidth and storage costs. To meet these requirements, the ITU-T and MPEG jointly introduced H.266, also known as Versatile Video Coding (VVC), which offers nearly 50% bitrate reduction compared to its predecessor H.265/HEVC.

Despite its superior compression performance, H.266 introduces significantly increased computational complexity due to advanced coding tools such as Quad-Tree plus Multi-Type Tree (QT+MTT) block partitioning, enhanced motion estimation, and sophisticated transform and prediction mechanisms. These features result in higher encoding and decoding latency, increased power consumption, and greater hardware resource utilization, making real-time and embedded implementations challenging. Consequently, improving the computational efficiency of H.266 without sacrificing compression performance has become an important research problem.

Recent studies on H.266 optimization primarily focus on algorithm-level simplifications and heuristic-based complexity reduction techniques. However, arithmetic-intensive operations within multiple block processing stages, such as transform computation, quantization, and prediction, continue to contribute significantly to overall processing delay. This creates an opportunity to explore alternative computational approaches that can enhance processing speed and efficiency at a lower architectural level.

Vedic Mathematics, an ancient system of computation based on efficient arithmetic principles, has gained attention in modern digital system design due to its ability to perform high-speed and low-complexity arithmetic operations. In parallel, Differential Multiple Coding (DMC) techniques exploit spatial and temporal redundancies by encoding differences between blocks rather than absolute values, thereby improving compression efficiency and reducing redundant processing.

Motivated by these observations, this project explores a novel performance enhancement approach for H.266 by integrating Vedic Mathematics-based arithmetic techniques within the multiple block processing architecture and incorporating a DMC encoder-decoder framework. The objective is to reduce computational complexity, minimize processing latency, and improve overall coding efficiency. This work focuses on conceptual analysis and system-level understanding, providing a strong foundation for future implementation and performance evaluation in real-time and hardware-based video coding systems.

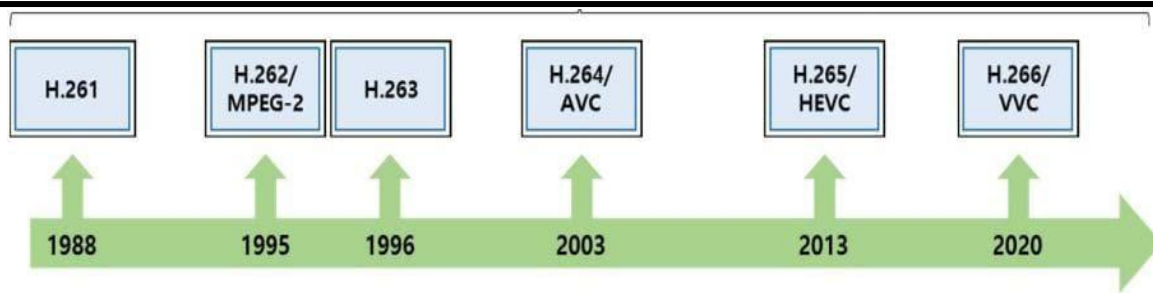


Fig. 1. Development of video coding standards (1988~2022).

This figure 1 shows the evolution timeline of international video compression standards developed by ITU-T and ISO/IEC over time.

It begins with H.261 (1988), the first practical digital video compression standard designed for video conferencing. This is followed by H.262/MPEG-2 (1995), widely used for DVD and digital television broadcasting, and H.263 (1996), which improved compression efficiency for low bit-rate applications. The introduction of H.264/AVC (2003) marked a major breakthrough, offering significantly better compression and becoming dominant in streaming and multimedia services. H.265/HEVC (2013) further improved efficiency, especially for high-definition and ultra-high-definition video. The latest standard, H.266/VVC (2020), achieves the highest compression efficiency, enabling advanced video applications such as 4K, 8K, and immersive media.

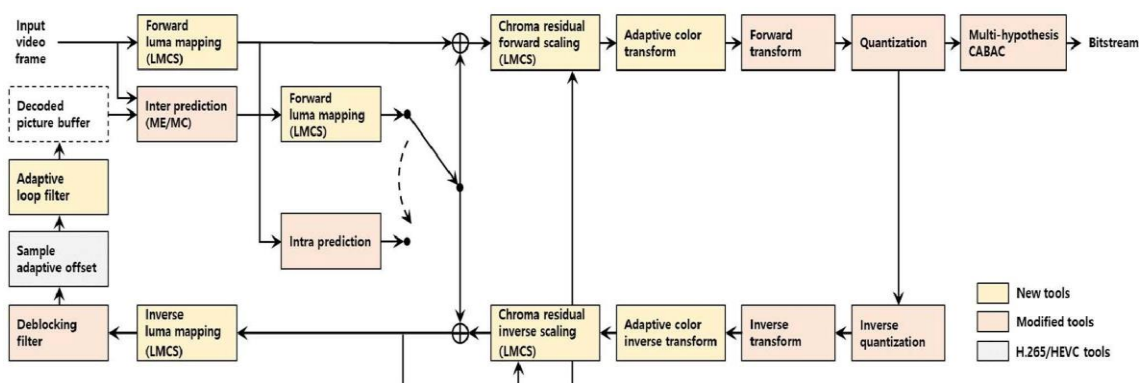


Fig. 2. Block diagram of H.266/VVC encoder

This figure 2 illustrates the overall block diagram of a modern video encoder (VVC/H.266) compared with HEVC (H.265), highlighting new and modified coding tools.

The input video frame is first processed using luma mapping with chroma scaling (LMCS), which improves perceptual quality by adapting luminance and chrominance values. The encoder then performs inter prediction (motion estimation/compensation) or intra prediction to remove temporal and spatial redundancies. The prediction residual is processed through adaptive color transforms and forward transforms, followed by quantization to reduce data precision. The quantized data is entropy-coded using multi-hypothesis CABAC to generate the compressed bitstream.

On the decoder side, inverse quantization and inverse transforms reconstruct the residual, followed by inverse color transform and inverse LMCS. Finally, in-loop filters such as deblocking, sample adaptive offset (SAO), and adaptive loop filtering refine the reconstructed frame before storing it in the decoded picture buffer. The color coding in the diagram distinguishes new tools, modified tools, and inherited HEVC tools, emphasizing VVC's enhancements for higher compression efficiency.

LITERATURE SURVEY

As stated in "[1]", the article focuses on video compression, a crucial technical aspect for the widespread use of digital video technology. It explains basic video coding concepts and provides detailed information on video formats and quality. The ideas behind H.264, such as its syntax, prediction methods, transform and coding techniques, and overall performance, are explained clearly and are easy to understand.

As in "[2]", the focus is on the fundamentals of image and video compression, along with various video coding standards such as JPEG, MPEG, H.261, H.263, and H.26L. Topics including motion estimation and compensation, pre- and post-processing techniques, and rate-distortion-complexity concepts are also covered. In addition, it provides information on video codec design and the platforms used for image and video compression.

As in "[3]", the paper focuses on the Discrete Cosine Transform (DCT) and its role in video compression. It presents the DCT formulas and discusses the key properties of the transform. The paper also compares DCT with other image transforms, such as the Karhunen–Loève Transform (KLT) and the Discrete Fourier Transform (DFT). In addition, a theoretical evaluation of DCT performance is carried out.

As in "[4]", the paper provides an overview of the technical features of H.264/AVC, describes the standard's profiles and applications, and outlines the history of its standardization process. The primary objectives of the H.264/AVC standardization effort are to achieve enhanced compression performance and to provide a network-friendly video representation that supports both conversational applications (such as video telephony) and non-conversational applications (including storage, broadcast, and streaming).

As in "[5]", the paper presents Context-Based Adaptive Variable-Length Coding (CAVLC), a significant feature of the H.264/AVC video coding standard. It highlights that a direct VLSI implementation of CAVLC, adapted from conventional run-length coding architectures, results in low throughput and inefficient resource utilization. To address this issue, the paper proposes an efficient CAVLC design.

As in "[6]", the paper proposes an implementation of a context-adaptive variable-length coder for an H.264 video encoder. The design supports user-defined video compression and is capable of processing high-resolution images up to 1024×768 pixels at a real-time frame rate of 25 frames per second. The variable-length coder is implemented using Verilog RTL coding. The achieved compression ratio exceeds 10, and the reconstructed image quality is better than 35 dB.

As in "[7]", the paper proposes a novel FPGA-based implementation of the core processing units—integer transform and quantization—for an H.264 video encoder. The system allows user-controlled compression and is capable of processing 1024×768 pixel color images in 4:2:0 format at 25 frames per second. The algorithms and architectures for integer transformation and quantization were designed and implemented using Verilog. The reconstructed image quality achieved is greater than 35 dB.

As in "[8]", the paper presents a comprehensive methodology for power reduction in video decoding across all design levels. Power consumption is optimized at the algorithmic, architectural, circuit, and physical levels through techniques such as parallelism, pipelining, and reduced memory access. A low-power bitstream residual decoder architecture for an H.264/AVC baseline decoder is proposed, along with the design and analysis of low-power building blocks. Various power reduction techniques are applied at both the architectural and circuit levels.

As in "[9]", the paper highlights the features of a new design that achieves approximately 50% bit-rate savings for equivalent perceptual quality compared to previous standards, particularly for high-resolution

video. It also emphasizes that, in the HEVC video coding standard, improving a single component alone does not significantly enhance codec performance; rather, performance gains are achieved through improvements across all processing blocks.

As in “[10]”, the paper proposes the design and implementation of a single-chip video decoder for portable multimedia applications. The chip employs a mixed hardware/software architecture to balance performance and flexibility, while also offering low power consumption and high adaptability.

As in “[11]”, the paper examines a VLSI implementation of a CAVLC decoder for H.264/AVC, including the underlying algorithm and the design of an efficient architecture. The proposed architecture is capable of decoding event syntax in a single cycle and operates at a maximum clock frequency of 125 MHz. These advantages demonstrate its suitability for high-throughput video applications.

As in “[12]” this work compares the quality, compression efficiency, and performance of H.265, H.264, and Motion JPEG video codecs. HEVC/H.265 provides the best video quality and compression efficiency but requires higher computational complexity. H.264 delivers moderate quality with the slowest encoding speed. Motion JPEG offers the fastest encoding time but produces lower video quality, especially when using the Open JPEG library. The study helps in selecting suitable video codecs based on quality, speed, and computational requirements.

As in “[13]” this paper presents a low-power H.265/HEVC Nova decoder designed for efficient video decoding in portable devices. Power optimization is achieved through architectural techniques such as pipelining, parallel processing, clock gating, and hierarchical memory organization. The design was implemented and verified on a Virtex-5 FPGA using Xilinx tools. Results show a significant reduction in gate count, area, and power consumption compared to previous designs. The H.265 standard delivers nearly the same video quality as H.264 at about half the bit rate. Although the deblocking filter increases complexity, the proposed architecture handles it effectively, with scope for further simplification in future work.

As in “[14]” The paper presents a hardware-efficient motion estimation architecture for the HEVC (H.265) standard, targeting the high computational complexity of video encoding. It focuses on implementing the Test Zone Search (TZS) algorithm with variable block sizes to reduce processing time. The proposed design is developed in VHDL and implemented on an FPGA platform. An embedded hardware/software co-design using a Nios II processor is used for validation. The architecture supports block sizes from 8×8 to 64×64 and achieves real-time performance. Experimental results show a throughput of up to 78 Mpixels/s at 100 MHz with reduced hardware cost.

As in “[15]” the paper presents a comparative analysis of modern video compression standards, including HEVC (H.265), AV1, and VVC (H.266). The study evaluates their compression efficiency based on factors such as video characteristics, quantization parameters, image quality, and spatio-temporal complexity (SI/TI). The results show that no single standard is universally superior, as performance varies with video content and resolution. AV1 demonstrates better compression efficiency than HEVC for SD, HD, and FHD video. Experimental results further indicate that VVC achieves the highest compression efficiency overall. Understanding the impact of SI and TI helps optimize encoding performance while reducing storage, transmission, and energy requirements.

PROPOUND HEVC

This survey identifies a significant research gap in arithmetic-level optimization and alternative coding paradigms for H.266/VVC. To address this gap, a novel research direction is proposed that integrates Vedic Mathematics-based arithmetic techniques into the multiple block processing architecture of H.266, along with a Differential Multiple Coding (DMC) encoder-decoder framework. The use of Vedic arithmetic is expected to reduce computational delay and hardware complexity, while the DMC approach aims to enhance compression efficiency by exploiting inter-block redundancies. This combined strategy

presents a promising pathway for achieving high-performance and low-power H.266 implementations in future real-time and embedded video systems.

CONCLUSION

This survey reviewed existing approaches for performance optimization and complexity reduction in the H.266/Versatile Video Coding (VVC) standard and highlighted the persistent challenges associated with its high computational complexity. The analysis indicates that most existing studies focus on algorithm-level optimizations, while arithmetic-level enhancements and alternative coding strategies remain largely unexplored. To address this gap, a promising research direction has been proposed that integrates Vedic Mathematics-based arithmetic techniques with a Differential Multiple Coding (DMC) encoder–decoder framework within the multiple block processing structure of H.266. This combined approach has the potential to reduce computational delay and improve compression efficiency, providing a strong foundation for future implementation and performance evaluation in real-time and resource-constrained video coding systems.

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