

Design Of A Charge-Pump Based, Phase Locked Loop(PLL) For Medical Applications

Vinayak, Divya, Sandyarani, Sai Prakash¹
Dr. Sagarkumar²

¹UG Students department of Electronics & Communication,

²Faculty, department of Electronics & Communication,
Lingaraj appa engineering college bidar, Karnataka.
Emails: svmbuyya@gmail.com

ABSTRACT

This paper presents the design and implementation of a low-power charge pump phase-locked loop (CP-PLL) intended for medical and biomedical electronic applications. The proposed PLL architecture consists of a phase frequency detector (PFD), charge pump (CP), loop filter (LF), voltage controlled oscillator (VCO), and frequency divider implemented in 90 nm CMOS technology. The system is designed to generate GHz-range output frequency from a MHz reference signal while maintaining low power consumption and reduced phase noise. A NAND/NOR-based PFD is employed to minimize dead zone and blind zone issues, and a current-starved ring VCO is utilized for low power and wide tuning range. The proposed CP-PLL architecture is suitable for implantable and wearable medical devices where power efficiency and frequency stability are critical.

Keywords— Phase-Locked Loop (PLL), Charge Pump, Voltage Controlled Oscillator, CMOS, Medical Applications, Frequency Synthesizer.

I. INTRODUCTION

Phase-Locked Loops (PLLs) are widely used in communication, biomedical, and integrated circuit applications for frequency synthesis, clock generation, and signal synchronization. With the rapid advancement of low-power electronics and implantable medical devices, the demand for stable and energy-efficient frequency synthesizers has significantly increased.

PLLs serve as essential timing and frequency control circuits that lock the output frequency and phase of a voltage-controlled oscillator (VCO) to a stable reference signal. They are extensively used in microprocessors, wireless communication systems, and biomedical monitoring devices. In medical applications, low power consumption, high stability, and low phase noise are critical design requirements.

This work focuses on the design of a charge pump-based PLL (CP-PLL) capable of generating GHz-range frequencies from a low-frequency reference input, making it suitable for biomedical and medical electronic systems.

II. LITERATURE REVIEW

Several researchers have contributed to the advancement of PLL design for low power and high-frequency applications. Previous studies have explored inverse sine phase detectors, multi-standard fractional PLLs, and noise-suppressed architectures for improved performance.

Recent works emphasize reducing current mismatch in charge pumps and minimizing phase noise in VCOs. Ring oscillators are commonly preferred for low-power applications due to their smaller area and lower supply

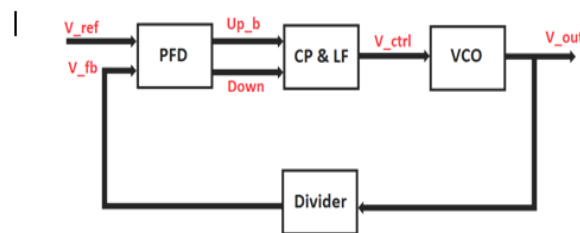
voltage requirements. Additionally, techniques such as calibrated loop filters and improved PFD architectures have been proposed to enhance lock time and stability.

However, many existing PLL designs suffer from high power consumption, dead zone in PFD, and charge pump current mismatch, which limit their suitability for medical applications.

III. METHODOLOGY

The chosen architecture is the charge pump phase locked loop with frequency divider that uses a fixed, nonprogrammable value. The block diagram of the PLL is shown in Figure below. It consists of a phase-frequency detector block (PFD) which cooperates with a charge pump (CP) and produces a square wave with duty cycle proportional to the phase error between the reference input (V_{ref}) and the feedback output (V_{fb}). This signal is converted to DC value by a second order loop filter, which consists of the charge pump and loop filter. The voltage V_{ctrl} is converted to current by the next block

and Voltage controlled oscillator (VCO) generates desired GHz output signal. Part of the output signal is fed back to the PFD through the frequency divider, whose division ratio is set to different multiple values using various dividers. The overall PLL system is as shown in the figure.

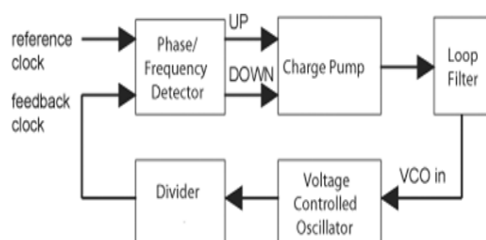


IV. PROPOSED CP-PLL ARCHITECTURE

The proposed architecture is a charge pump phase-locked loop consisting of the following major blocks:

- Phase Frequency Detector (PFD)
- Charge Pump (CP)
- Loop Filter (LF)
- Voltage Controlled Oscillator (VCO)
- Frequency Divider (FD)

The PFD compares the phase and frequency of the reference signal and feedback signal and generates UP and DOWN pulses. These pulses control the charge pump, which converts them into current signals. The loop filter then converts the current into a control voltage (V_{ctrl}) that tunes the VCO. The output of the VCO is fed back through a frequency divider to complete the closed-loop system.



1 PHASE FREQUENCY DETECTOR

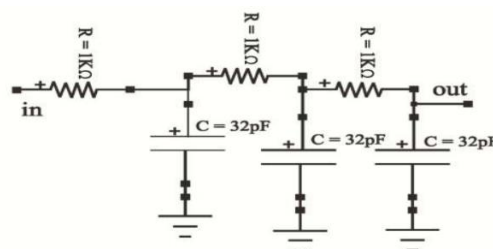
In recent times PLL has become an inevitable part of any communication system and is irreplaceable. Many modifications have been successfully proposed by researchers to get the best out of PLL. These modifications come at a different level of abstraction. One can do the complete architectural redesign or redesigning only a particular block of PLL. PFDs being the first block that takes the input and the reference frequency and decides the generation of stable frequency. They also help us in defining the locking status of the signal. In this chapter, a NAND based PFD circuit has been proposed. The proposed PFD works well for the medical band of frequencies thus making it very suitable for PLLs in the biomedical field.

2 CHARGE PUMP (CP)

A charge Pump is a circuit that injects or pulls out a charge for a controlled amount of time. In the CP-PLL it is placed after the PFD and before the loop filter. The combined effect of all the three elements is to produce a voltage that is proportional to the phase error between the VCO's output and the reference. Charge pump along with the loop filter averages out the voltage given out of the PFD thus creating the control voltage for the VCO. The charge pump is basically a combination of two current sources and two switches that switches the sources. We have implemented Gate Switched Charge Pump in our project. Charge Pump is the circuit which transmits the voltage signals in the PFD to the corresponding current signals as accurately as possible. In other words, CP is used to sink and source current into a LF based on the digital error pulses from the PFD. Figure 4.1 shows the CP. The CP circuit consists of two switched current sources with magnitudes of I_{UP} and I_{DOWN} , and in most cases both the sources are identical. Hence, $I_{UP} = I_{DOWN} = I_{CP}$. If the error signal from the PFD is an UP signal, then the CP pumps charge when I_{UP} is connected to the positive supply rail. On the other hand, if the error signal from the PFD is a DOWN signal, then the CP removes charge when I_{DOWN} is connected to the negative supply rail. The current sources are separated by two switches S1 & S2.

3 LOOP FILTER

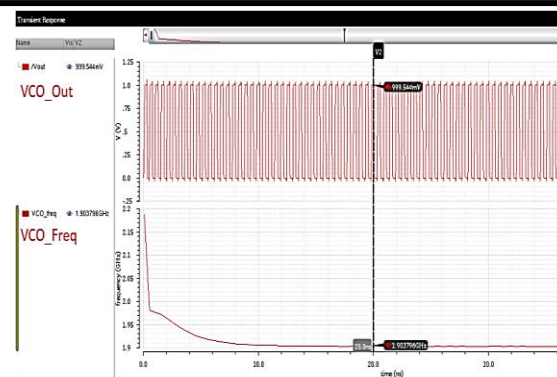
A Loop filter is the Low Pass Filter (LPF) which incorporates error current to generate VCO control voltage and restrains the noise and unwanted phase detector. The filter shown in Figure 5.9 alters the ability of the loop to change frequencies instantly. If the filter receives a low cut off frequency, then the changes in tune voltage take place slowly.



4. VOLTAGE CONTROLLED OSCILLATOR (VCO)

A current-starved ring oscillator is selected due to its low power consumption and suitability for biomedical applications. The VCO consists of multiple delay stages forming a feedback loop that produces oscillations.

The oscillation frequency is controlled by the control voltage (V_{ctrl}), which adjusts the delay of each stage. Compared to LC oscillators, ring VCOs offer:

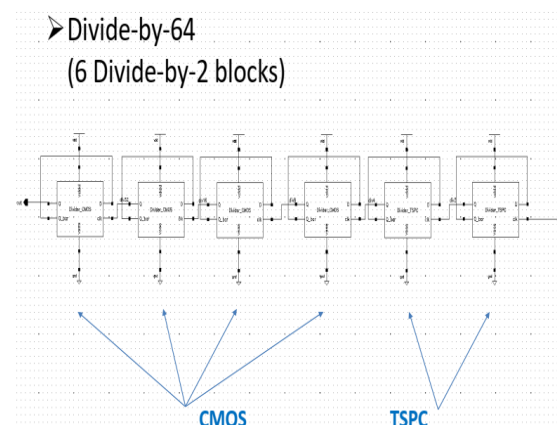


- Lower power consumption
- Smaller chip area
- Wider tuning range

These characteristics make them ideal for implantable medical devices.

5 FREQUENCY DIVIDER

A True Single-Phase Clock (TSPC) flip-flop based frequency divider is used to scale down the VCO output frequency. The divider ensures synchronization between the reference and feedback signals and supports high-speed operation with low power consumption.



V. CONCLUSION AND FUTURE WORK

Designing a low power PLL is very crucial in medical applications. For the medical band application, designing an PLL that consumes minimal power is a challenging task. By using the concept of NAND based PFD, loop filter and VCO with divider, the PLL has been designed. The design of low power ADPLL for medical based applications ensuring minimal power consumption was the main objective of this work. Using the theory and circuits developed, a full low power PLL was developed. The architecture was designed in the 90 nm CMOS process.

Five objectives were met in the due course of the entire project. In the first objective, a PFD circuit was designed, and its performance was assessed. In the second objective, a charge pump was designed, third objective focused on the design of oscillators, fourth objective focused on divider and finally fifth objective involved the integration of the entire blocks to get the full PLL for medical applications.

VI. FUTURE WORK AND SCOPE

Many improvements can still be applied to the design, like reducing power consumption by investigating other LC VCO and charge pump topologies. Also, using synchronous counters and CML flipflops in the divider can help reduce the accumulated jitter in the divider path. The PLL output frequency can be increased to few more giga hertz making it a versatile block for other communication-based applications as well.

REFERENCES

- [1] D. Fathi and A. G. Nejad, "Ultra-low power, low phase noise 10 ghz lc vco in the subthreshold regime," *Circuits and Systems*, vol. 4, no. 04, p. 350, 2013
- [2] Bhardwaj, Monika, Sujata Pandey, and Neeta Pandey. "A novel design of a 1 GHz phase locked loop with improved lock time for fast frequency acquisition." *International Journal of Computer Aided Engineering and Technology* 17.2 (2022): 192-207.
- [3] Dutta, Debojyoti, et al. "Exploring the Landscape of Phase-Locked Loop Architectures: A Comprehensive Review." *IEEE Access* (2024).
- [4] Bae, J., Radhapuram, S., Jo, I., Kihara, T. and Matsuoka, T. (2015), A low voltage design of controller-based ADPLL for implantable biomedical devices, in *Proceedings of the 'IEEE Biomedical Circuits and Systems Conference (BioCAS)'*, pp. 1-4
- [5] Balikai, V. and Kittur, H. (2020). 'A CMOS implementation of controller based all digital phase locked loop (ADPLL)', *Circuit World* May 2020
- [6] Cheng, K., Tsai, Y., Lo, Y. and Huang, J. (2011), 'A 0.5-V 0.4-2.24 GHz Inductorless phase-locked loop in a system-on-Chip', *IEEE Transactions on Circuits and Systems I: Regular Papers* 58(5), 849-859
- [7] Erfani-Jazi, H. R. and Ghaderi, N. (2015), 'A divider-less, high speed and wide locking range phase locked loop', *AEU - International Journal of Electronics and Communications* 69(4), 722-729
- [8] Ferriss, M. and Flynn, M. P. (2007), A 14 mW Fractional-N PLL modulator with an enhanced digital phase detector and frequency switching scheme, in 'Proceedings of 2007 IEEE International Solid-State Circuits Conference, Digest of Technical Papers' pp. 352-608
- [9] Fuketa, H., O'uchi, S. and Matsukawa, T. (2017), 'Fully integrated, 100-mV minimum input voltage converter with gate-booster charge pump kick-started by LC oscillator for energy harvesting', *IEEE Transactions on Circuits and Systems II: Express Briefs* 64(4), 392-396.