

CMOS Design & Implementation Of High Speed & Stable 1KB SRAM Cell For Space Related Applications

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ABSTRACT

Static Random Access Memory (SRAM) plays a crucial role in modern high-speed processors due to its low latency and fast access time. However, achieving high speed, low power consumption, and stability simultaneously remains a major challenge in nanoscale CMOS technologies, especially for space applications where reliability is critical. This paper presents the design and implementation of a high-speed and stable 1 KB SRAM using a 6T SRAM cell in 90 nm CMOS technology operating at 1 V supply. The proposed design includes peripheral circuits such as pre-charge circuitry, sense amplifier, row decoder, column decoder, write driver, and 32×32 memory array. Static Noise Margin (SNM) is analyzed using the butterfly curve for stability evaluation. The simulation results demonstrate improved access speed, reduced delay, and enhanced read/write performance suitable for high-speed.

Keywords— SRAM, CMOS, 6T SRAM, Sense Amplifier, SNM, High-Speed Memory, Low Power VLSI.

INTRODUCTION

Semiconductor memories have a significant role has most fundamental units in VLSI layout. It is the most important unit in SOC and contain memories inclusive of flash memory, read only memory (ROM), static random access memory (SRAM) and dynamic random access memory (DRAM). SRAM which is kind of memory used in computer that keeps its information stored as long as power is supplied. It is described as “static” because unlike dynamic RAM which require frequent refreshing to maintain its information. SRAM is commonly utilized as a memory for input/output operations in computer systems and as high-speed cache memory in CPU. Compared to DRAM, it is more costly and faster and also more dependable, uses less power and has a higher access time. This makes SRAM cells a fundamental building block of modern computing systems and a key technology for achieving high-speed data processing. SRAM is made of flip flops which are electrical circuits storing a bit of information. Four to six transistors make up each flip-flop, allowing them to maintain their value until power is turned off. SRAM is used in variety of computer systems and electronics including routers, phone switches and other networking equipment, as a result of its many benefits. SRAM is typically found in cache memory in microprocessors and other types of memory in devices. SRAM can be designed using BJT's however, power loss in switching is larger. SRAM is now created utilizing MOSFET's which reduces power loss in switching. In this nanoscale era, the static or leaky power usage of CMOS devices predominate over the dynamic power dissipation. Whenever power is consumed in device it generates heat that heat has to get out of the device and that can create problems for small form factor device.

LITERATURE SURVEY

Previous works have explored SRAM designs across different technology nodes to improve delay and power consumption. Technology scaling reduces delay but introduces stability and process variation issues. Alternative topologies such as 8T and 5T SRAM improve specific parameters but increase area and complexity.

Several studies emphasized Static Noise Margin (SNM) as a key stability metric. However, many designs lack:

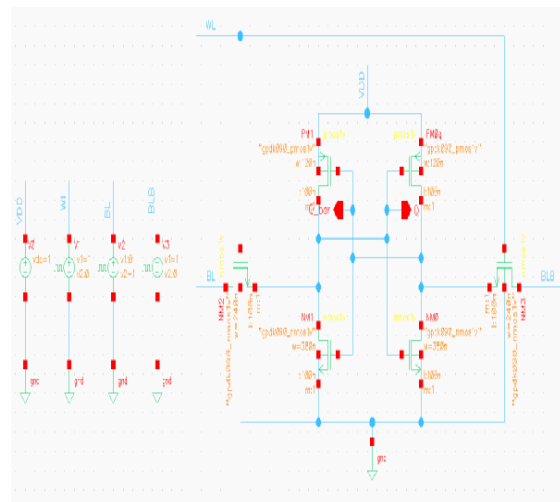
- Optimized access time

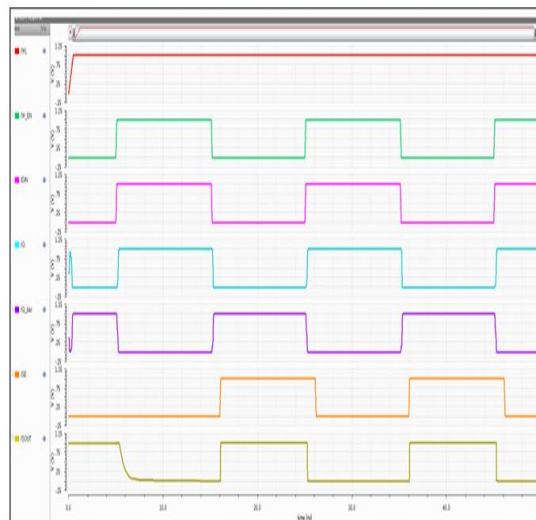
- Detailed peripheral circuit implementation
- Process variation tolerance
- Balanced speed–power trade-off

This motivates the proposed high-speed 1 KB SRAM design with improved throughput and stability.

METHODOLOGY

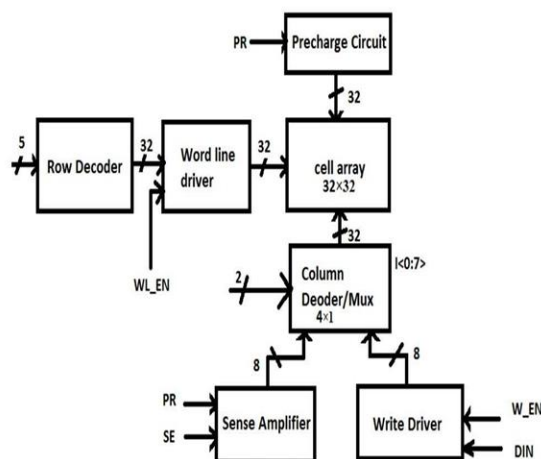
As mentioned in the introduction, the main 1- bit 6T SRAM is designed by placing two CMOS cross coupled inverters which works as a latch. These two inverters are used to latch the data to be saved. Latch perform different operations, i.e. Read, Write & Hold. This latch is operated by internal pulse provided to it. Additionally, to its two access transistors are also used to provide access to BL and BLB (both BL & BLB works according to WL). The basic structure of a 6T SRAM memory cell.





BLOCK DIAGRAM OF 1KB SRAM CELL

1-kb SRAM block structure which includes Cell Array, decoder, sense amplifier, write driver, column mux, precharge circuitry, address latch and read and write control as the peripheral circuit to the SRAM cell array. Since the memory core trade performance and reliability in reduction area, memory design relies exceedingly on the peripheral circuitry to recover both speed and electrical integrity. While the design of the core is dominated by technological consideration and is largely beyond the scope of the circuit designer, it is in the design of the periphery where a good designer can make an important difference. Generally, for smaller memory designs monolithic architectures are preferred, but in the Design of bigger memories monolithic architecture will not give efficient performance. The frequency of operation of the circuit is reduced by a factor of two as the number of rows doubles. Similarly, the frequency of memory, reduced by a factor of four as the number of 42 columns doubles, hence in bigger memory designs memory portioning technique is used which is known as memory banking.



Precharge circuit is used to pre-charging the both bit lines voltages to supply voltage and pre-charging operation should perform before every write and read operation. Figure 3.4 shows the pre-charge circuit which consists of pull up PMOS transistors and an equalizer which is used to equalize the voltage on both bit lines. The pull up PMOS transistors are controlled by PR signal i.e. The Transistor M3 shown in the schematic of Pre-charge is an equalizer which is used to equalize the voltage on both bit lines. Pre-charge circuit should provide large driving current to drive the bit lines which are having large parasitic capacitances, so the transistor sizes of pre-charge circuit need to be increased. Therefore, size of transistors used in precharge circuit is large. When the

precharge signal is low bit lines get charged and when it goes high bit lines becomes floating. Test Circuit for the precharge circuit

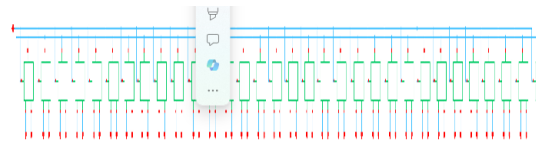
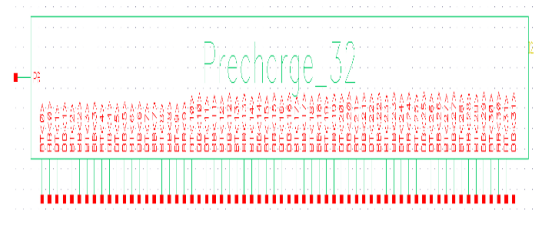
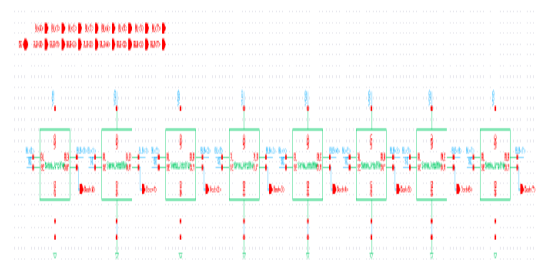


Fig 3.4.2. Test Circuit of 32-bit Precharge Circuit



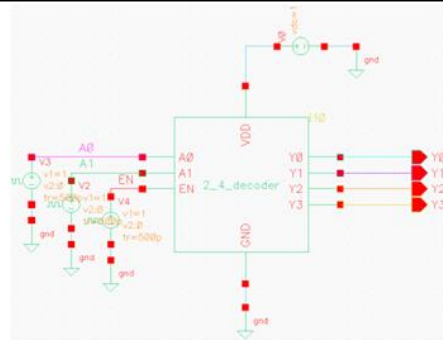
DESIGN OF SENSE AMPLIFIER CIRCUIT

Sense Amplifiers plays a crucial role in the design of memories to achieve performance, reliability and functionality of memory circuits. Figure 3.5 shows the design of sense amplifier circuit. Normally sense amplifiers perform various operations like voltage amplification, reduction in delay, power reduction and restoration of original signal. Generally, sense amplifiers are used in the memories to speed up the read operation. Sense amplifier takes the small signal difference bit line voltage as input and gives full swing single ended output. Access time and power consumption of memory is affected by the sense amplifier hence the performance of memory is improved by reducing both sensing delay and power dissipation.



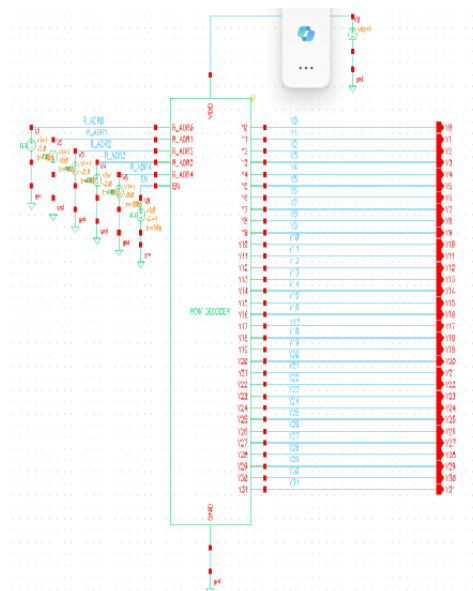
DESIGN OF 2:4 DECODER

Whenever a memory allows for random address based access, address decoders must be present. The design of these decoders has a substantial impact on the speed and power consumption of the memory. Since only one transition determines the decoder speed, it is interesting to evaluate other circuit implementation. Dynamic logic offers a better alternative. A first solution is presented in Fig. 3.6, where the transistor diagram of decoder is depicted. Notice that this structure is identical to the NOR ROM array, differing only in the data patterns. The same structure can be used to build 5:32 decoder for 32x32 memory array. Test circuit for 2:4 decoder is shown in fig 3.6.1 and the simulation



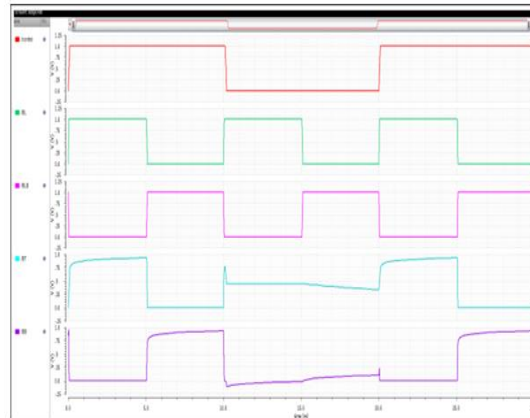
DESIGN OF 5:32 ROW DECODER

Row decoder, whose task is to empower one memory row out of 2^M , where M is the width of particular fields in address word. When the number of inputs is more than or equal to four then the speed of operation of the decoder is affected so pre-decoders are to be used which reduces the large fan-in. The structure of 2:4 decoder is used to build 5:32 decoder.



DESIGN OF COLOUMN MULTIPLEXER

For 1-kb 8-bit SRAM block, Array is of size 32x32 and we have to select 8 out of 32 bit lines for that 4:1 column mux is used. 2:4 decoder is needed to select one of the select lines of column mux. It is better to design 4:1 mux using transmission gate logic. NMOS pass transistor logic mux works very well during write cycle as one of the bit line need to discharge to ground and NMOS is good to transfer zero logic. Fig 3.8 shows the schematic of column mux for write operation and the waveform



The stability of SRAM cell can be decided by mostly three parameters i.e. Static Noise Margin (SNM), Read Margin (RM) and Write Margin (WM). cell ratio (CR) and pull-up ratio (PR) are two parameters which effects the above three parameters.

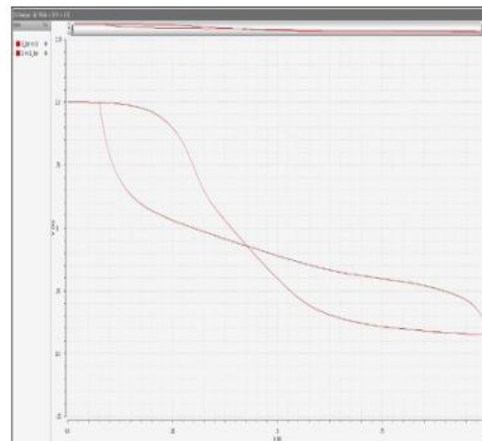
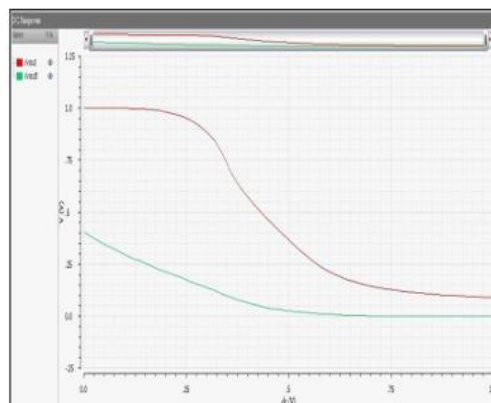
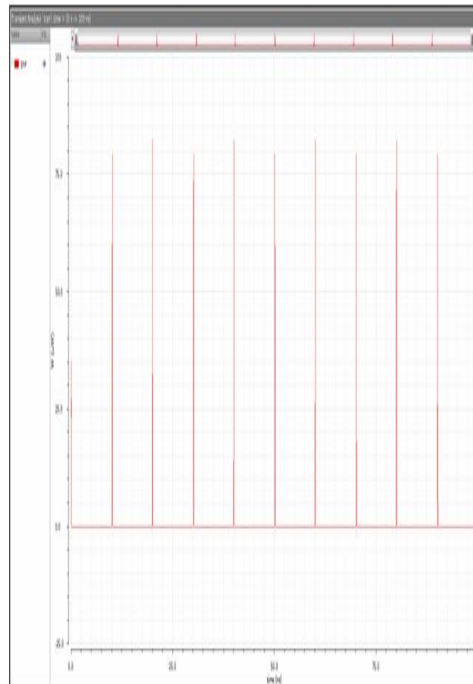


Fig 4.2: Butterfly Curve Analysis for Read Operation.



POWER ANALYSIS

- **SRAM (Static Random-Access Memory)** consumes power in two main ways: **Dynamic Power:** This is the dominant power consumption during read and write operations. It occurs when transistors in the SRAM cell switch states. In this proposed work 82.23uW dynamic power is consumed
- **Static Power:** This is the leakage current that flows even when the SRAM is not actively reading or writing data. It's a continuous power drain. In this proposed work 36.617nW dynamic power is consumed.



The proposed work involves the performance analysis of a 1kb Static Random-Access Memory (SRAM) using 1-bit 6T SRAM cells. The simulations were conducted using Spectre, a popular tool for circuit simulation, and the memory is designed using a 90nm CMOS technology node. The primary focus of the project is on achieving high speed, and thus, attention is given to analyzing the delay to ensure that the memory array operates within specified speed requirements. In this proposed work successfully achieved its objectives, focusing on the development of a high-speed 1kb SRAM using single bit 6T SRAM cells in a 90nm CMOS technology node. The proposed work placed significant emphasis on achieving high-speed operation. Various design techniques, including transistor sizing, topology optimization, and circuit-level innovations, were employed to minimize access time and enhance overall speed. In the stability analysis of a single 6T SRAM cell, the design achieves a Read Noise Margin of 70.578 mV and a Write Noise Margin of 595 mV for a supply voltage of 1V. These parameters are crucial indicators of the stability and reliability of the memory cell. The Read Noise Margin ensures reliable read operations by providing a sufficient voltage difference between the stable states, while the Write Noise Margin ensures robust write operations by allowing for sufficient voltage margins to write data reliably into the memory cell. Overall, the analysis demonstrates that the designed 6T SRAM cell meets the stability requirements for reliable memory operations.

By achieving adequate noise margins and ensuring stability, the memory array can operate effectively within the specified speed requirements, thereby enhancing its performance and reliability in practical applications.

FUTURE SCOPE

The future works that can be conducted for manufacturing of 2kb ,1MB chip using designed 1-kb block. For that 1MB memory need to design using 1-kb block so that operating frequency will be near to 1kb design. Whereas the design of bigger memories beyond the range of Mb such as Gb can be designed by using scripting languages like Perl and SKILL because the layout design of such a bigger memory could not be drawn with the hands of a

man. Hence in industries the bigger memory designs can be automated by using scripting languages to achieve better performance. By carefully considering these strategies, challenges, and future trends, which create a roadmap for designing larger memories using smaller building blocks while striving to maintain performance characteristics comparable to the original 1kb design. The optimal approach will depend on specific application requirements, technology limitations, and cost constraints.

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